AMENDMENTS TO THE DRAWINGS:

Please amend Figures 26 to add the appropriate lead lines, in compliance with 37 C.F.R. § 1.84(q), as shown in the attached drawing Replacement Sheet attached hereto.

Attachments: Drawing Replacement Sheet (Figure 26).

REMARKS

In the outstanding Office Action, the Examiner objected to the drawings; objected to claims 4, 5, 38, and 39; rejected claims 3-5, 34, and 37-39 under 35 U.S.C. § 112, first paragraph; rejected claims 1, 2, 35, and 36 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,306,940 to Yamazaki ("Yamazaki"); rejected claims 3, 4, 34, and 37 under 35 U.S.C. § 102(b) as being anticipated by newly cited U.S. Patent No. 5,567,962 to Miyawaki et al. ("Miyawaki"); and rejected claim 5 under 35 U.S.C. § 103(a) as being unpatentable over Miyawaki.

By this amendment, Applicants have amended claims 4, 5, 38, and 39. Claims 1-5, and 34-39 remain pending in this application.

I. Objections to the drawings

In the Office Action, the Examiner objected to the drawings, stating that "it is unclear what are locations of reference numerals 61, 62, 63, and 64," and "Fig. 26 should show the elements for reference numerals 61-64." Office Action, page 2. Applicants hereby propose amending Figure 26 as shown in the attached drawing Replacement Sheet, to add the appropriate lead lines, in compliance with 37 C.F.R. § 1.84(q). Applicants respectfully request that the Examiner approve the amendment to Figure 26, and withdraw the objection to the drawings.

II. Objections to the claims

Regarding the Examiner's objection to claims 4, 5, 38, and 39, Applicants disagree with the Examiner's assertions as set forth in the Office Action. In order to address the Examiner's concerns and expedite prosecution, however, Applicants have

amended claims 4, 5, 38, and 39. Accordingly, Applicants respectfully request that the objection to claims 4, 5, 38, and 39 be withdrawn.

III. Objections under 35 U.S.C. § 112, first paragraph

Regarding the rejection of claims 3-5, 34, and 37-39 under 35 U.S.C. § 112, first paragraph, Applicants disagree with the Examiner's assertions because the Examiner's position does not conform to standard U.S. practice. Accordingly, Applicants respectfully traverse this rejection.

It is Applicants' understanding that the written description issues raised by the Examiner on pages 3-4 of the Office Action are due to the Examiner's failure to appreciate that "the element isolating insulating film having a top surface which is *lower* than a top surface of said semiconductor layer," as recited in claim 3 (emphasis added), and as shown in Figures 17A-19C, is related to the rest of the Figures and their respective descriptions. Accordingly, the Examiner apparently asserts that any claim elements not shown in Figures 17A-19C, and the description of those figures, are not supported in the specification.

The M.P.E.P. provides that in order to satisfy the written description requirement of 35 U.S.C. § 112, first paragraph:

> an applicant must convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention, and that the invention, in that context, is whatever is now claimed. An applicant shows possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as *words*, structures, *figures*, diagrams, and formulas that fully set forth the claimed invention ... [p]ossession may be shown in a variety of ways including ... *the disclosure of drawings*. (Internal citations

omitted) (emphasis added). M.P.E.P. § 2163.02, 8th Ed. (Rev. 3), October, 2005.

Accordingly, Applicants can satisfy the written description requirement by having described the claimed invention through "words" or "drawings." Initially, Applicants note that the specification at, for example, page 42, lines 4-5, describes a metal gate electrode. Moreover, the specification at page 54, lines 14-16, describes in Figure 12, a step amount δ, which is the height "of the top surface position P_{Si} relative to the top surface position $P_{ins.}$." The specification, at page 54, lines 10-12 further states that the structure as shown in Figure 12 "is formed using, for example, *any of the first to tenth embodiments*" (emphasis added). Moreover, at page 55, lines 16-19, the specification describes an embodiment related to Figure 12, wherein "a MOS transistor of step amount $\delta \leq 0$ is of a type where the top surface position $P_{ins.}$ is at the same level as the top surface position P_{Si} or is *below* the same" (emphasis added). Accordingly, Applicants have described an embodiment wherein a structure formed as in "any of the first to tenth embodiments" can have a step amount δ, "where the top surface position $P_{ins.}$ is at the same level as the top surface position P_{Si} or is below the same." Figures 17A-19C thus show an embodiment wherein a step amount $\delta \leq 0$, and accordingly, can also be formed using "any of the first to tenth embodiments."

Accordingly, the Examiner has made an improper rejection under 35 U.S.C. § 112, first paragraph. Therefore, Applicants respectfully request that the Examiner withdraw the rejection of claims 3-5, 34, and 37-39 under 35 U.S.C. § 112, first paragraph.

IV. Rejections under 35 U.S.C. § 102(b)

Regarding the rejection of claims 1-4, and 34-37, Applicants disagree with the Examiner's assertions and conclusions as set forth in the Office Action.[1] Accordingly, Applicants respectfully traverse this rejection.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference ... [t]he identical invention must be shown in as complete detail as is contained in the . . . claim." M.P.E.P. § 2131 8th Ed. (Rev. 3), October, 2005 (internal citations omitted).

A. Yamazaki

Independent claims 1 and 2 each recite a combination including "the element isolating insulating film having a top surface projecting upward above a top surface of said semiconductor region." Yamazaki fails to teach at least this element. The Examiner alleges that silicon oxide films 113 and 116a and BPSG film 115c (as shown in Figs. 8A-8F) constitutes the "element isolating insulating film," and that silicon oxide films 113 and 116a and BPSG film 115c further "partition[s] said semiconductor layer into a plurality of element regions." Office Action, pages 4-5.

Contrary to the Examiner's characterization, Yamazaki teaches "an element isolation region in which a combination of a LOCOS type field oxide film and a U-trench isolation region buried with an insulating film such as BPSG film ... is used." Yamazaki, col. 10, lines 37-40 (emphasis added). Moreover, "silicon oxide film 113 is to prevent

[1] The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether any such statement is identified herein, Applicants decline to automatically subscribe to any statement of characterization in the Office Action.

boron and/or phosphor from diffusing from the BPSG film to the silicon substrate," and "silicon oxide film 116a prevents diffusion of boron and phosphor from the BPSG film 115c during subsequent various heat treatments and serves as a protection film." Yamazaki, col. 11, lines 14-16, 44-48. Silicon oxide films 113 and 116a thus are not used to isolate or insulate element regions in semiconductor layer 103. Accordingly, Yamazaki only teaches that BPSG film 115c can be used as an element insulating film. Because only BPSG film 115c can even be arguably construed as corresponding to Applicants' claimed "element isolating insulating film," Applicants further note that Figures 8A-8F of Yamazaki clearly show BPSG film 115c being below the top of semiconductor layer 103.

Yamazaki thus fails to teach a combination including "the element isolating insulating film having a top surface projecting upward above a top surface of said semiconductor region," as recited in claims 1 and 2. Accordingly, claims 1 and 2 are allowable over Yamazaki, and claims 35 and 36 are allowable at least due to their respective dependence on claims 1 and 2.

B Miyawaki

Regarding the rejection of claims 3, 4, 34 and 37 under 35 U.S.C. § 102(b) as being anticipated by newly cited Miyawaki, Applicants disagree with the Examiner's characterization of this reference, and believe that the reference cannot anticipate at least independent claim 3 because it fails to teach each and every element of the claim. For example, Miyawaki fails to teach a combination including at least "an element isolating insulating film *provided in the trench* for partitioning said semiconductor layer into a plurality of element regions," as recited in claim 3 (emphasis added).

At page 6 of the Office Action, the Examiner characterizes Miyawaki as teaching "a trench (the area occupied by layer [1091'])," and "an element isolating insulating film [1091'] provided in the trench." Miyawaki teaches that element 1091' constitutes a "field oxidized film." Miyawaki, col. 17, lines 7-8. Applicants note that even if field oxidized film 1091' could be reasonably construed to constitute Applicants' "element isolating insulating film," as recited in claim 3, contrary to the Examiner's characterization, the area occupied by field oxidized film 1091' is not a trench. As shown in Figures 16-17 of Miyawaki, silicon oxide film 1062 is formed by selectively etching silicon oxide film 1060. Miyawaki further teaches, with reference of Figures 32 and 33, "[t]he manufacturing process ... is the same as that of the first embodiment," and "[a]n interlayer insulator is formed utilizing TEOS, and a SiO_2 layer 1091 is formed by etchback." Miyawaki, col. 16, lines 58-65. SiO_2 layer 1091 in Figure 32 is thus formed similarly to silicon oxide film 1062 in Figure 17.

Miyawaki then teaches that "[a]fter the silicon nitride film and then the pad oxide film are removed, the wafer is washed and *gate oxidation is then conducted* so as to shape the field oxidized film, as indicated by 1091' of FIG. 33." Miyawaki, col. 17, lines 5-8 (emphasis added). Miyawaki thus fails to teach the formation of a trench, and accordingly cannot be construed as teaching "an element isolating insulating film provided in the trench for partitioning said semiconductor layer into a plurality of regions," as recited in claim 3 (emphasis added).

Moreover, even if field oxidized film 1091' could be reasonably construed to constitute Applicants' "element isolating insulating film," Figure 33 shows that an interior side of field oxidized film 1091' is curved. Accordingly, an interface between field

oxidized film 1091' and the region occupied by p+ layer 1013, p layer 1016, and p- layer 1021 (collectively, an element region) is curved. Since the region between field oxidized layer 1091', p+ layer 1013, p layer 1016, and p- layer 1021 is curved and not perpendicular, Miyawaki thus also fails to teach "said element isolating insulating film and each of said element regions make an interface which is substantially *perpendicular* to the top surface of said semiconductor layer," as further recited in claim 3 (emphasis added). Accordingly, Miyawaki fails to teach each and every element recited in claim 3, and claim 3 is allowable over Miyawaki. Moreover, claims 4, 34, and 37 are also allowable over Miyawaki at least due to their dependence on claim 3.

For at least the foregoing reasons, Applicants submit that the references fail to teach each and every element recited in claims 1-4, and 34-37. Accordingly, Applicants respectfully request that the Examiner withdraw the rejection of claims 1-4, and 34-37 under 35 U.S.C. § 102(b).

V. Rejection under 35 U.S.C. § 103(a)

Applicants respectfully traverse the rejection of claim 5 under 35 U.S.C. § 103(a) because a *prima facie* case of obviousness has not been established. To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. *See* MPEP §2143.03, 8th Ed. (Rev. 3), October, 2005. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three

requirements must " be found in the prior art, and not be based on applicant's disclosure." *See* MPEP § 2143, 8th Ed. (Rev. 3), October, 2005. The Examiner has failed to establish a *prima facie* case of obviousness because, at a minimum, Miyawaki fails to teach or suggest each and every element required by claim 5.

Claim 5 depends from claim 3, and thus requires all of the elements recited in claim 3. As discussed above, Miyawaki fails to teach or suggest a combination including at least "an element isolating insulating film *provided in the trench* for partitioning said semiconductor layer into a plurality of element regions," as recited in claim 3, and required by claim 5 (emphasis added). At page 10 of the Office Action, the Examiner states that

> [i]t would have been obvious for the difference in height from said substrate between the top surface position of said semiconductor layer and the top surface position of said element isolating film is substantially at least a junction depth of said source/drain region because it depends on the resistance of the source/drain region.

Although Applicants disagree with this statement, this statement does not constitute a teaching of "an element isolating insulating film provided in the trench for partitioning said semiconductor layer into a plurality of element regions," as recited in claim 3, and required by claim 5.

Accordingly, Miyawaki also fails to teach or suggest every element required by claim 5. Applicants therefore respectfully request that the Examiner withdraw the rejection of claim 5 under 35 U.S.C. § 103(a).

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: January 30, 2006

By: RMB for Reg #31,744
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